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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheets

of 1

| <i>Complete If Known</i> | |
|--------------------------|----------------------|
| Application Number | 10/780,143 |
| Filing Date | February 17, 2004 |
| First Named Inventor | Alexander Barr et al |
| Group Art Unit | 2811 |
| Examiner Name | |
| Attorney Docket Number | SC13265TP |

U. S. PATENT DOCUMENTS

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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

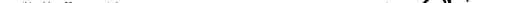
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| Examiner Initials* | File No. 1 | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. |
|  | BB | M. SHIMA et al - "<100> Channel Strained - SiGe p-MOSFET with Enhanced Hole Mobility and Lower Parasitic Resistance" (2002 Symposium on VLSI Technology Digest of Technical Papers, pg 94-95 |
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EXAMINER: Initial U reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation, if not in conformance and not considered. Include copy of this form with next communication to applicant.

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|--|---|----|---|--------------------------|--------------------------|
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i> | | | | <i>Complete if Known</i> | |
| Sheet | 1 | of | 1 | Application Number | 101-780,143 |
| | | | | Filing Date | FEBRUARY 17, 2004 |
| | | | | First Named Inventor | Alexander L. Barr et al. |
| | | | | Group Art Unit | 2823 |
| | | | | Examiner Name | W. DAVID COLEMAN |
| | | | | Attorney Docket Number | SCI13265TP |

| NON PATENT LITERATURE DOCUMENTS | | | |
|---|-----------------------|---|----------------|
| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
|  | AC | LANGDO et al., "Preparation of Novel SiGe-Free Strained Si on Insulator Substrates," AMBERWAVE SYSTEMS CORP., SALEM, NH, 2 pgs. | |
|  | AD | MATSUMOTO et al., "Novel SOI Wafer Engineering Using Low Stress and High Mobility CMOSFET with <100>Channel for Embedded RF/Analog Applications," IEEE, pp. 663-666 (2002). | |
|  | AE | SAYAMA et al., "Effect of <100> Channel Direction for High Performance SCE Immune pMOSFET with Less Than 0.15µm Gate Length," IEEE, 4 pgs., (1999). | |
|  | AF | AOKI et al., "Optimum Crystallographic Orientation of Submicrometer CMOS Devices Operated at Low Temperatures," IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. ED-34, NO. 1, JANUARY 1987, pp. 52-57. | |

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|--------------------|---|-----------------|-----------------|
| Examiner Signature |  | Date Considered | October 4, 2005 |
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